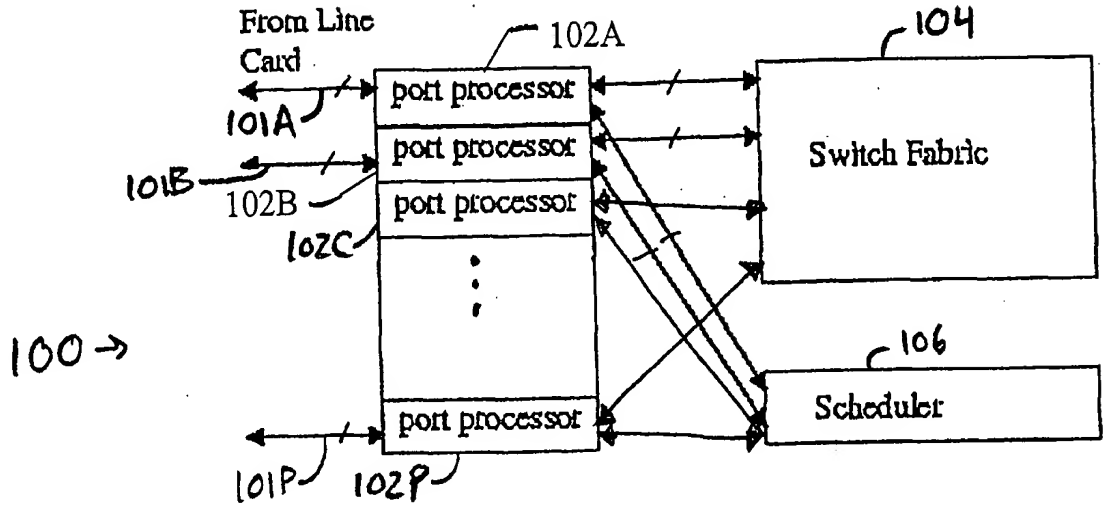
From Line Card
102A
104
port processor
port processor
port processor
port processor
Switch Fabric
101A
101B
102B
102C
100
106
Scheduler
101P
102P

Figure 1.

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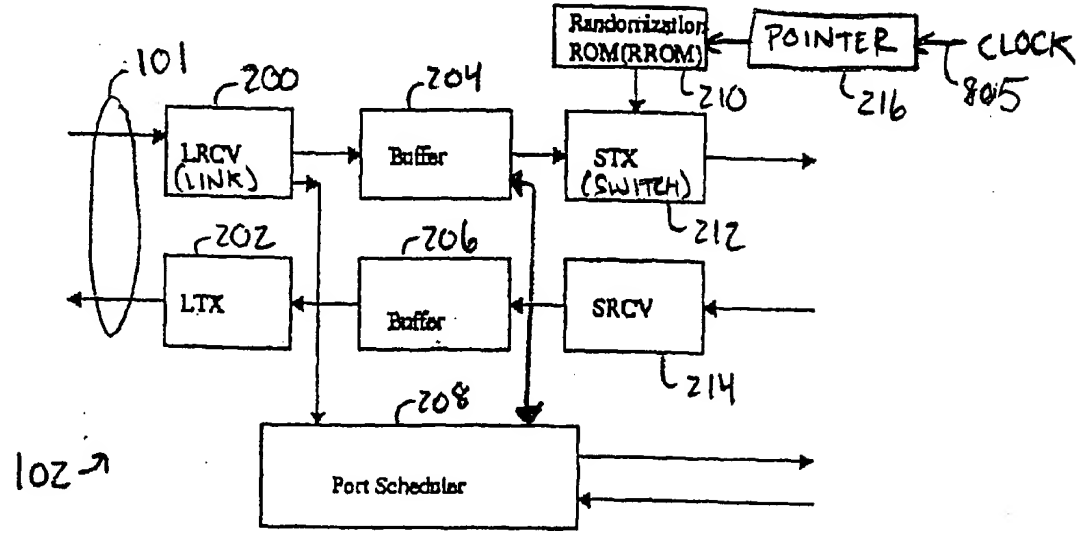


FIGURE 2

FIGURE 3A

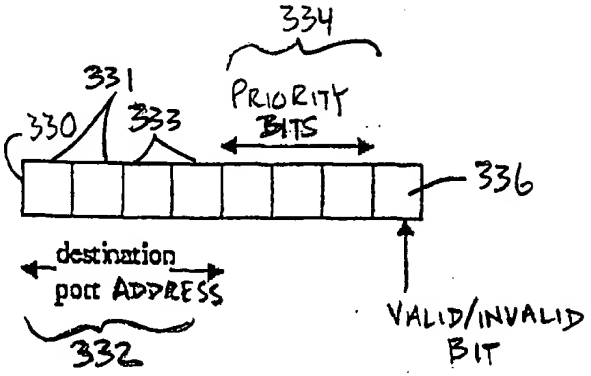
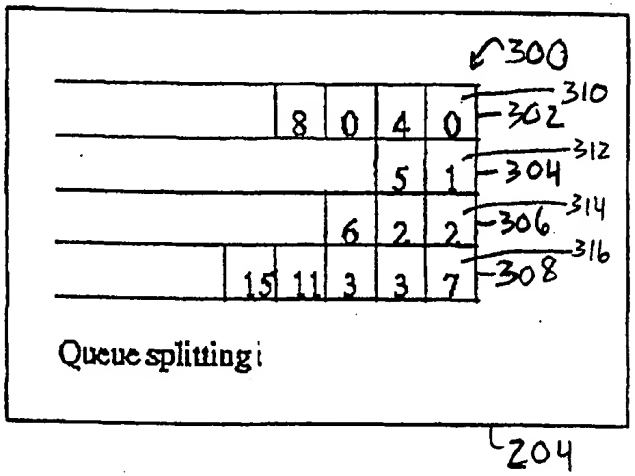


FIGURE 3B



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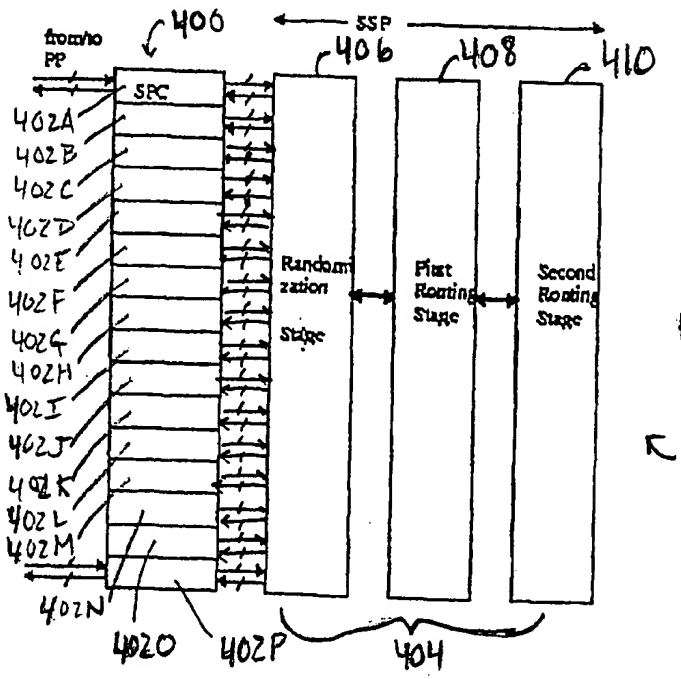

FIGURE 4

106

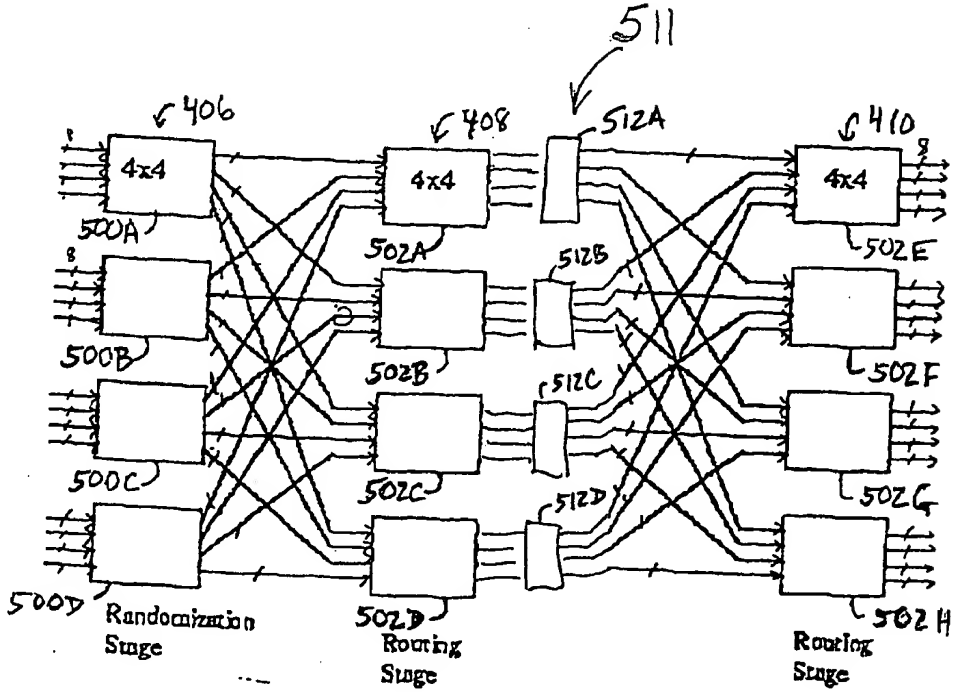
511
406
408
410
512A
4x4
4x4
4x4
500A
502A
512B
502E
500B
502B
512C
502F
500C
502C
512D
502G
500D
502D
502H
Randomization Stage
Routing Stage
Routing Stage

FIGURE 5

404

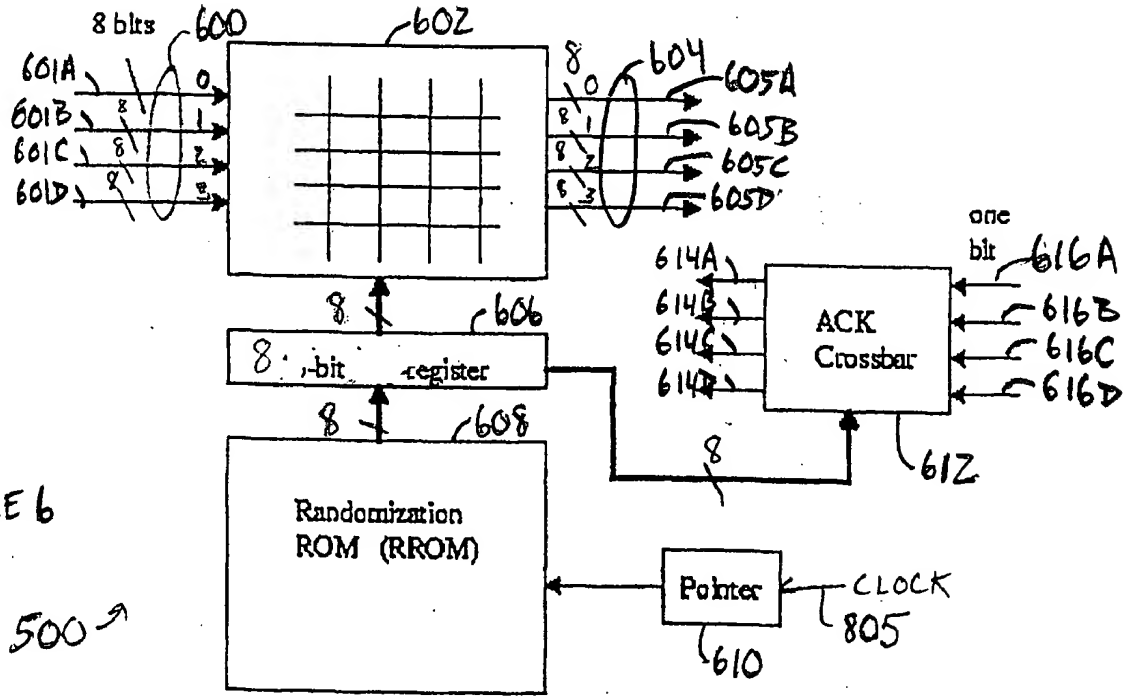
8 bits
600
602
601A
601B
601C
601D
0
1
2
3
8
604
605A
605B
605C
605D
614A
614B
614C
614D
ACK
Crossbar
one
bit
616A
616B
616C
616D
612
606
8-bit register
608
Randomization
ROM (RROM)
Pointer
CLOCK
805
610
500

FIGURE 6

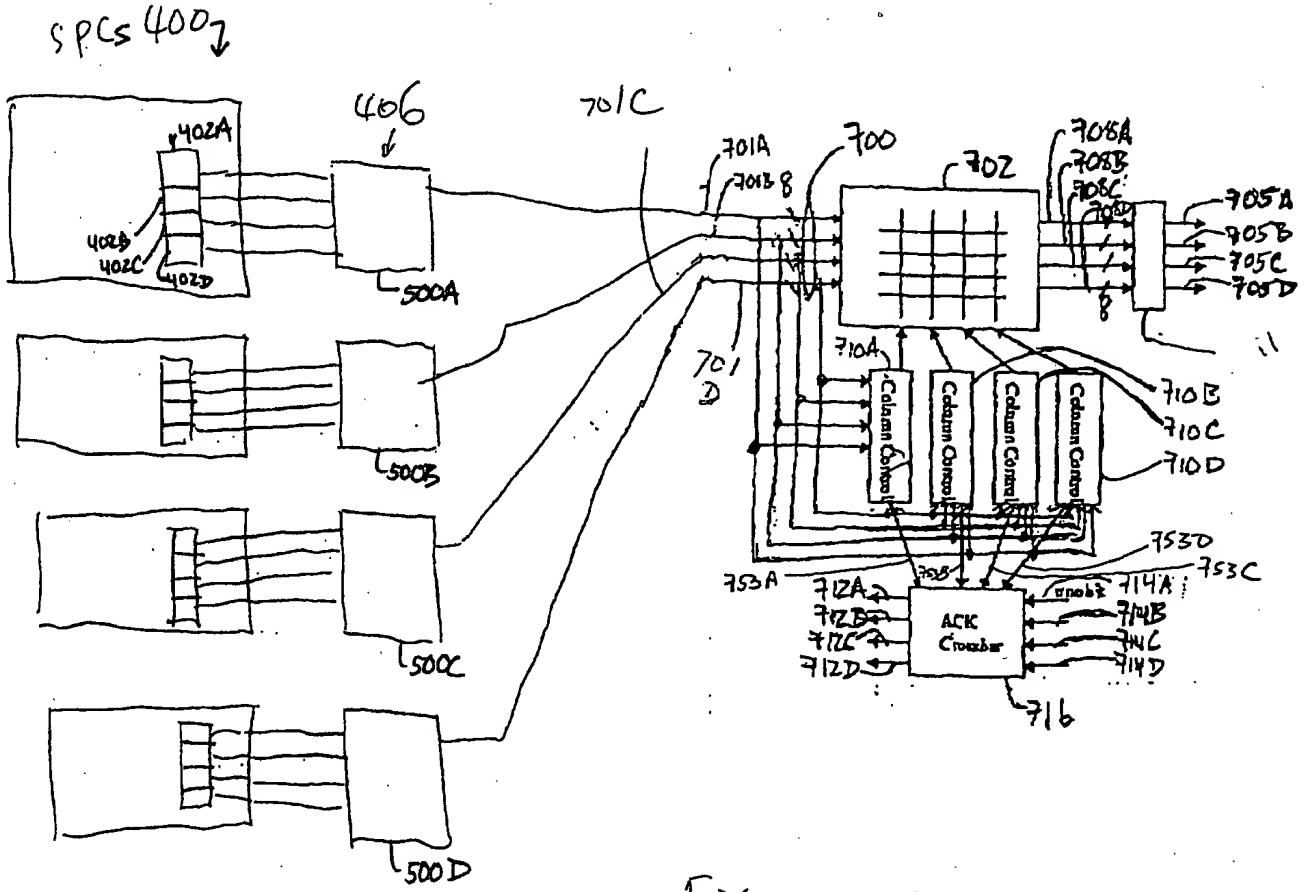
SPCs 400
406
701C
402A
402B
402C
402D
500A
500B
500C
500D
701A
701B
700
702
708A
708B
708C
708D
705A
705B
705C
705D
701D
710A
710B
710C
710D
Column Control
Column Control
Column Control
Column Control
753D
753C
753A
712A
712B
712C
712D
ACK Crossbar
714A
714B
714C
714D
716

Figure 7A

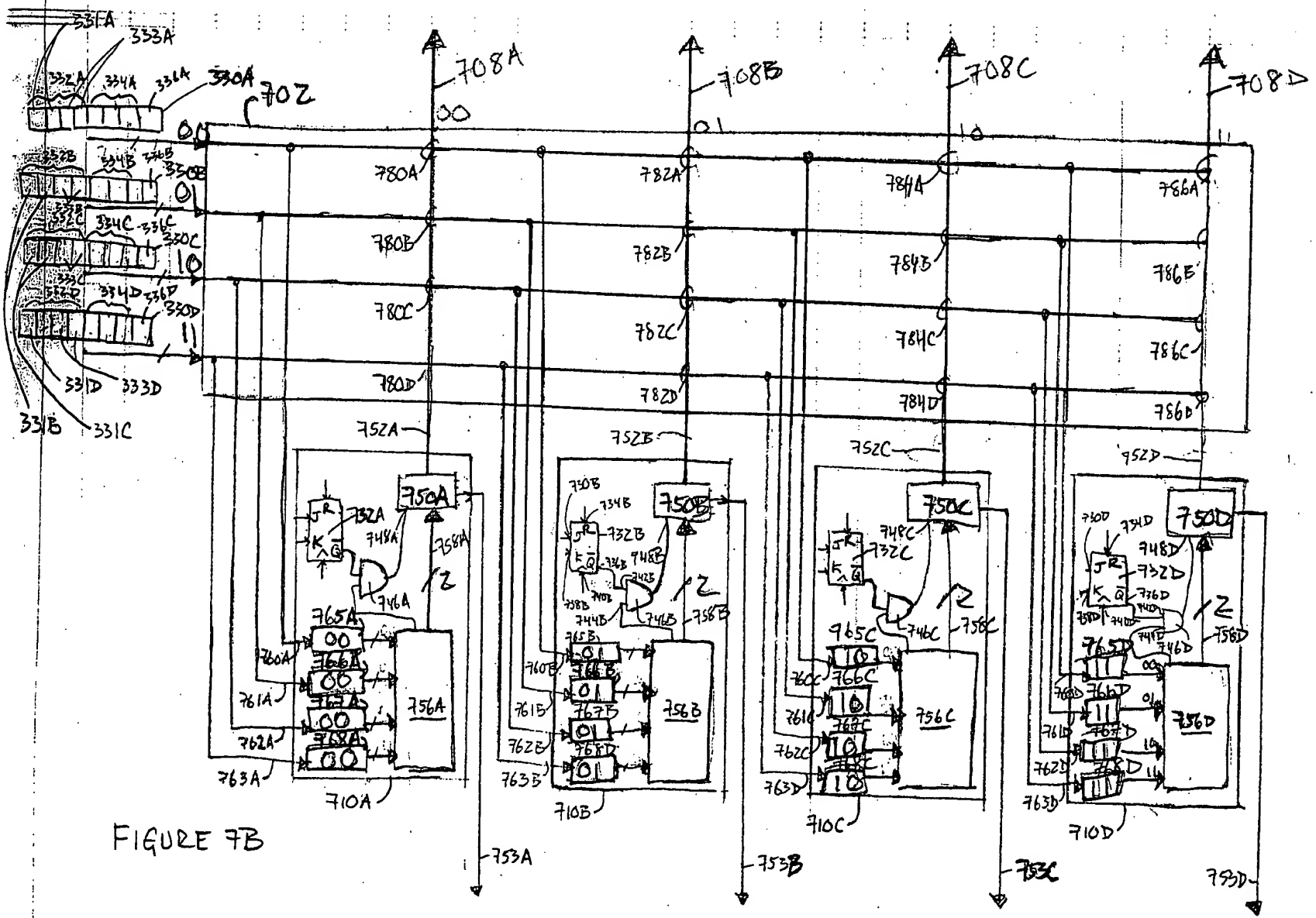
331A
333A
332A
334A
336A
330A
702
708A
708B
708C
708D
00
01
10
11
332B
334B
336B
330B
332C
334C
336C
330C
332D
334D
336D
330D
331D
333D
331B
331C
780A
780B
780C
780D
782A
782B
782C
782D
784A
784B
784C
784D
786A
786B
786C
786D
752A
752B
752C
752D
750A
750B
750C
750D
732A
732B
732C
732D
734B
734D
748A
748B
748C
748D
746A
746B
746C
746D
758A
758B
758C
758D
765A
765B
765C
765D
766A
766B
766C
766D
768A
768B
768C
768D
760A
760B
760C
760D
761A
761B
761C
761D
762A
762B
762C
762D
763A
763B
763C
763D
756A
756B
756C
756D
710A
710B
710C
710D
753A
753B
753C
753D

FIGURE 7B

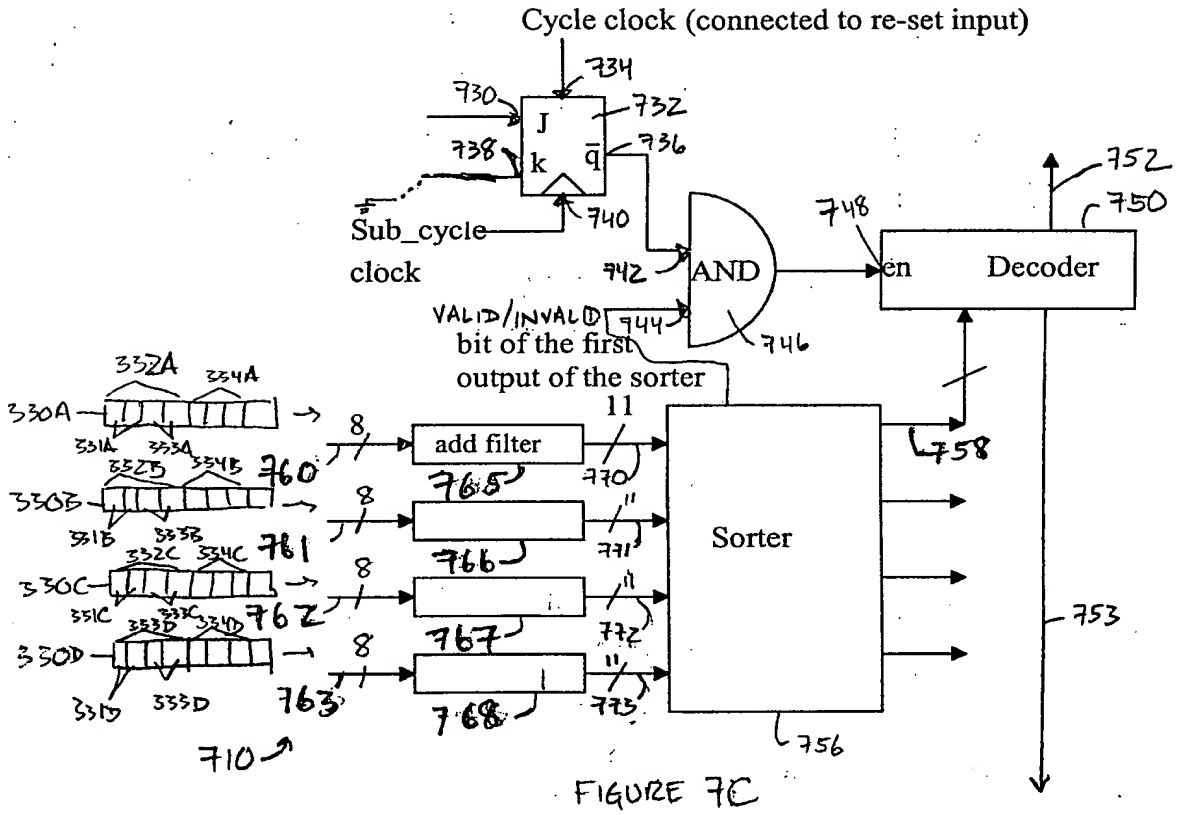
Cycle clock (connected to re-set input)
734
730
J
732
738
k
q
736
740
Sub_cycle clock
742
AND
748
en
Decoder
752
750
VALID/INVALID bit of the first output of the sorter
744
746
332A
334A
330A
331A
333A
334B
760
330B
331B
333B
332C
334C
761
330C
331C
333C
762
330D
331D
333D
763
710
8
add filter
765
770
11
766
771
767
772
768
773
Sorter
758
753
756

FIGURE 7C

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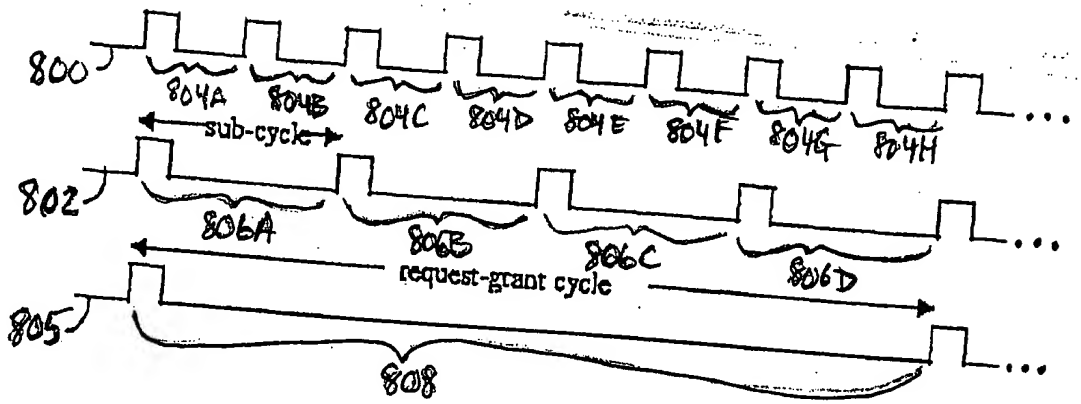
FIGURE 8



DOE2TD 82589260

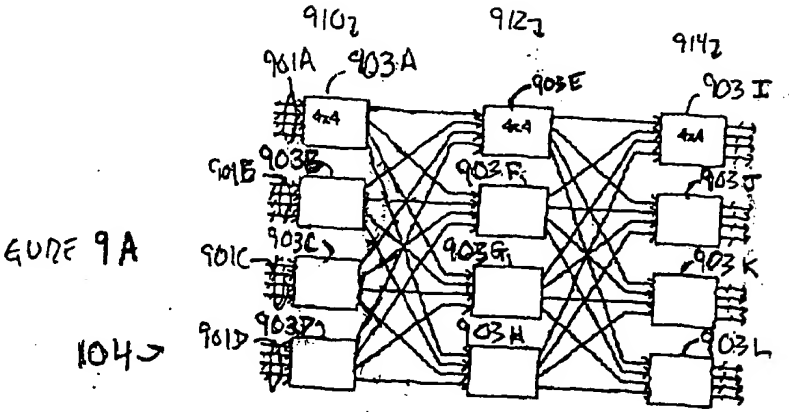
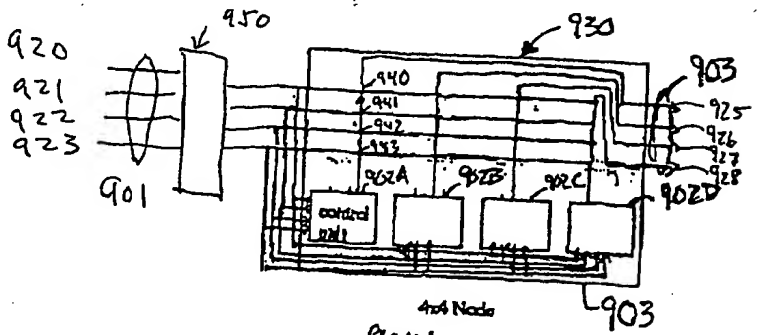


FIGURE 9A

Figure 9B



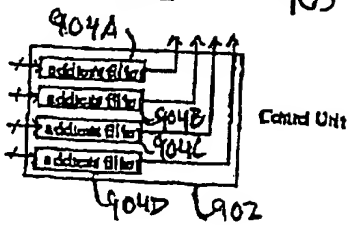


FIGURE 9C